REMARKS

This Amendment is in response to the Office Action of June 30, 2000. Claims 16-34 are currently pending in the application. Each of claims 16-34 stands rejected. Reconsideration of the application is respectfully requested in light of the amendments and remarks presented herein.

The Office' reminder regarding the direction of product-by-process claims to the product *per se* is gratefully acknowledged. Accordingly, the arguments presented herein relating to rejections under 35 U.S.C. §§ 102 and 103(a) are limited to elements of the product, and do not extend to the processes recited in the claims.

Objections to the Drawings

The drawings were objected to as being informal. Formal drawings are being transmitted herewith under separate cover. In addition, FIGs. 22 and 23 were objected to as being photographs for which a Petition pursuant to 37 C.F.R. § 1.84(b) has not yet been granted. It is respectfully submitted that such a Petition is not required as the Office, in 1998, issued an Interim Waiver of 37 C.F.R. 1.84(b) for Petitions to Accept Black and White Photographs and Advance Notice of Change to M.P.E.P. 608.02, a copy of which is enclosed herewith.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 16-18, 21-23, and 26-28 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 16-18, 21-23, and 26-28 have each been amended to remedy the deficiencies cited in the outstanding Office Action. Specifically, occurrences of the phrase "storage poly" have been replaced with the phrase "storage poly structure" and the phrases "desired position" and "desired areas" have been replaced with the more definite phrase "at least a portion".

With respect to the rejection of claim 27 as reciting "the storage poly layer" without providing proper antecedent basis, this rejection is respectfully traversed. The indicated location of claim 27 sets forth "a storage poly layer" rather than "the storage poly layer".

For these reasons, it is respectfully requested that the 35 U.S.C. § 112, second paragraph, rejections of claims 16-18, 21-23, and 26-28 be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 16, 21, 26, and 31-34 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,686,747 to Jost et al. (hereinafter "Jost").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Jost teaches a capacitor structure for a semiconductor device that includes, among other things, a polysilicon storage cell structure, or first electrode, with hemispherical grain (HSG) polysilicon, a capacitor dielectric formed over the HSG polysilicon, and a second electrode overlying the capacitor dielectric. Jost also teaches methods for fabricating the capacitor structure, as well as intermediate structures that are formed while the capacitor structure is under fabrication.

Independent claim 16, as amended and presented herein, recites, among other things, a storage poly structure that includes hemispherical grain polysilicon, a mask over the hemispherical grain polysilicon, through which only portions of the hemispherical grain polysilicon layer are exposed, and recesses in the storage poly structure.

By way of contrast with amended claim 16, Jost lacks disclosure of a mask formed over the hemispherical grain polysilicon of the storage poly structure thereof, that the hemispherical grain polysilicon is exposed through the mask, or that the storage poly structure beneath the hemispherical grain polysilicon includes recesses.

For these reasons, it is respectfully submitted that Jost does not anticipate the structure recited in amended claim 16. Accordingly, it is respectfully requested that the Office withdrawn the 35 U.S.C. § 102 rejections of claim 16.

Independent claims 21 and 26, as amended and presented herein, respectively recite, among other things, a semiconductor capacitor and a semiconductor memory cell, each of which includes a storage poly structure with hemispherical grain polysilicon thereon, recesses formed in the storage poly structure, a dielectric material over the storage poly structure and lining the recesses in the storage poly structure, and a cell poly located over the dielectric material.

Jost does not disclose a semiconductor capacitor or a semiconductor memory cell that includes a storage poly structure that includes recesses therein and hemispherical grain polysilicon thereover, or dielectric material over the storage poly structure and lining the recesses thereof.

Therefore, it is respectfully submitted that Jost does not anticipate each and every element of either amended claim 21 or amended claim 26, and requested that the section 102(e) rejections of these claims be withdrawn.

Independent claim 31, as amended and presented herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. The recesses comprise a plurality of contiguous mesas forming a maze-like structure.

Jost does not disclose a semiconductor capacitor storage poly with downwardly extending recesses that form a plurality of contiguous mesas. Rather, Jost discloses a storage poly layer that is formed from or lined with hemispherical grain polysilicon and, thus, has nonplanar surfaces rather than downwardly extending recesses.

Claim 32 is allowable as depending from claim 31, and further because Jost does not disclose mesas that extend in the X, Y, and Z coordinates.

Independent claim 33, as amended and presented herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. The recesses comprise a plurality of contiguous webs forming a maze-like structure.

Jost does not disclose a semiconductor capacitor storage poly with downwardly extending recesses that form a plurality of contiguous webs. Rather, Jost discloses a storage poly layer that

is formed from or lined with hemispherical grain polysilicon and, thus, has nonplanar surfaces rather than downwardly extending recesses.

Claim 34 is allowable as depending from claim 33, and further because Jost does not disclose webs that extend in the X, Y, and Z coordinates.

Rejections Under 35 U.S.C. § 103(a)

Claims 16-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jost in view of U.S. Patent 5,623,243 to Watanabe et al. (hereinafter "Watanabe").

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Jost teaches a capacitor structure for a semiconductor device that includes, among other things, a polysilicon storage cell structure, or first electrode, with hemispherical grain (HSG) polysilicon, a capacitor dielectric formed over the HSG polysilicon, and a second electrode overlying the capacitor dielectric. Jost also teaches methods for fabricating the capacitor structure, as well as intermediate structures that are formed while the capacitor structure is under fabrication.

Watanabe teaches capacitor devices that include polysilicon layers with uneven surfaces. The uneven surfaces of the polysilicon layers are formed with hemispherical grain polysilicon.

Independent claim 16, as amended and presented herein, recites, among other things, a storage poly structure that includes hemispherical grain polysilicon, a mask over the hemispherical grain polysilicon and through which only portions of the hemispherical grain polysilicon are exposed, and recesses formed in the storage poly structure.

Neither Jost nor Watanabe, taken either alone or in combination, teaches or suggests a storage poly structure that includes hemispherical grain polysilicon, a mask over the

hemispherical grain polysilicon and through which only portions of the hemispherical grain polysilicon layer are exposed, or that the storage poly structure beneath the hemispherical grain polysilicon includes recesses formed therein.

Accordingly, it is respectfully submitted that amended independent claim 16 is allowable over Jost and Watanabe taken alone or together. Therefore, it is respectfully requested that the section 103(a) rejection of claim 16 be withdrawn.

Claims 17-20 are each allowable, among other reasons, as depending either directly or indirectly from claim 16, which should be allowed.

Independent claims 21 and 26, as amended and presented herein, respectively recite, among other things, a semiconductor capacitor and a semiconductor memory cell, each of which includes a storage poly structure with hemispherical grain polysilicon thereon, recesses formed in the storage poly structure, a dielectric material over the storage poly structure and lining the recesses in the storage poly structure, and a cell poly located over the dielectric material.

Neither Jost nor Watanabe, taken alone or in combination, teaches or suggests a semiconductor capacitor or a semiconductor memory cell that includes a storage poly structure with recesses formed therein and hemispherical grain polysilicon thereon or a dielectric material lining the recesses in the storage poly structure.

Accordingly, it is respectfully submitted that amended independent claims 21 and 26 are each allowable over Jost and Watanabe, taken alone or in combination. Thus, it is respectfully requested that the Office withdraw the 35 U.S.C. § 103(a) rejection of independent claims 21 and 26.

Claims 22-25 are each allowable, among other reasons, as depending either directly or indirectly from claim 21, which should be allowed.

Claims 27-30 are each allowable, among other reasons, as depending either directly or indirectly from claim 26, which should be allowed.

Independent claim 31, as amended and presented herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. The recesses comprise a plurality of contiguous mesas forming a maze-like structure.

By way of contrast with claim 31, neither Jost nor Watanabe, alone or in combination, teaches or suggests a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. Nor does either Jost or Watanabe teach or suggest recesses that form a maze-like structure. Rather, the teachings of Jost and Watanabe are limited to storage poly layers that have uneven surfaces imparted to them by hemispherical grain polysilicon.

Claim 32 is allowable as depending from claim 31, and further because Jost and Watanabe both lack any teaching or suggestion of a storage poly structure with mesas that extend in the X, Y, and Z coordinates.

Independent claim 33, as amended and presented herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. The recesses comprise a plurality of contiguous webs forming a maze-like structure.

In contrast to claim 31, Jost and Watanabe, taken either alone or in combination, do not teach or suggest a semiconductor capacitor storage poly that includes downwardly extending recesses formed therein. Moreover, neither of these references includes any teaching or suggestion that these recesses form a maze-like structure. Rather, the teachings of Jost and Watanabe are limited to storage poly layers that have uneven surfaces imparted to them by hemispherical grain polysilicon.

Claim 34 is allowable as depending from claim 33, and further because Jost and Watanabe both lack any teaching or suggestion of a storage poly structure with mesas that extend in the X, Y, and Z coordinates.

New Claims 35-41

New claims 35-41 have been added. It is respectfully submitted that none of claims 35-41 introduces new matter. Support for each of the elements recited in new claims 35-41 is found in the originally filed specification, for example, in claims 16-34.

Claim 35 includes limitations similar to the product limitations of amended claim 16, and is allowable over the cited references for the same reasons as amended claim 16. Claim 36 is allowable as depending from claim 35.

Claim 37 includes limitations similar to the product limitations of amended claims 21 and 26. It is respectfully submitted that claim 37 is allowable for the same reasons provided above with respect to amended claims 21 and 26.

New independent claim 38 recites a semiconductor memory cell structure that includes a storage poly structure, a plurality of recesses extending into the storage poly structure, and a dielectric layer substantially coating an upper surface of the storage poly structure and substantially lining each of the plurality of recesses. As neither Jost nor Watanabe disclose, teaches, or suggests a semiconductor memory cell structure with a storage poly structure including recesses extending thereinto and a dielectric layer coating an upper surface of the storage poly structure, as well as the recesses therein, it is respectfully submitted that new claim 38 is allowable over these references.

Claims 39-41 each depend from claim 38, and are each allowable at least for that reason.

CONCLUSION

It is respectfully submitted that each of claims 16-34 is allowable. An early indication of the allowability of these claims and a notice that the case has been passed for issuance are respectfully solicited. If any issues preventing the allowance of any of claims 16-34 remain that might be resolved by way of a telephone conference, the Office is respectfully invited to contact the undersigned at the telephone number provided below.

Respectfully submitted,

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Date: September 28, 2000

BGP/sls:djp

Enclosure: Interim Waiver of 37 C.F.R. 1.84(b) for Petitions to Accept Black and White Photographs and Advance Notice of Change to M.P.E.P. 608.02

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